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IP-Centric and Software Defined Programming of Heterogeneous Systsems

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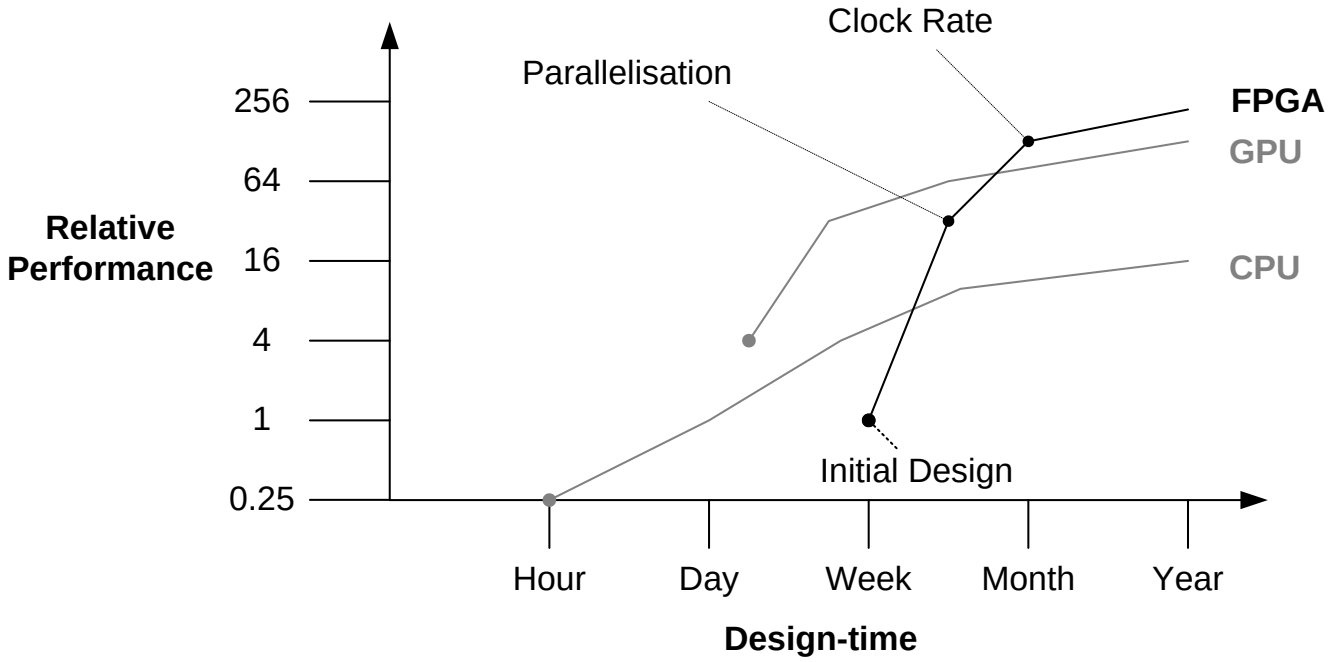
Sr. Product Marketing Manager, Xilinx

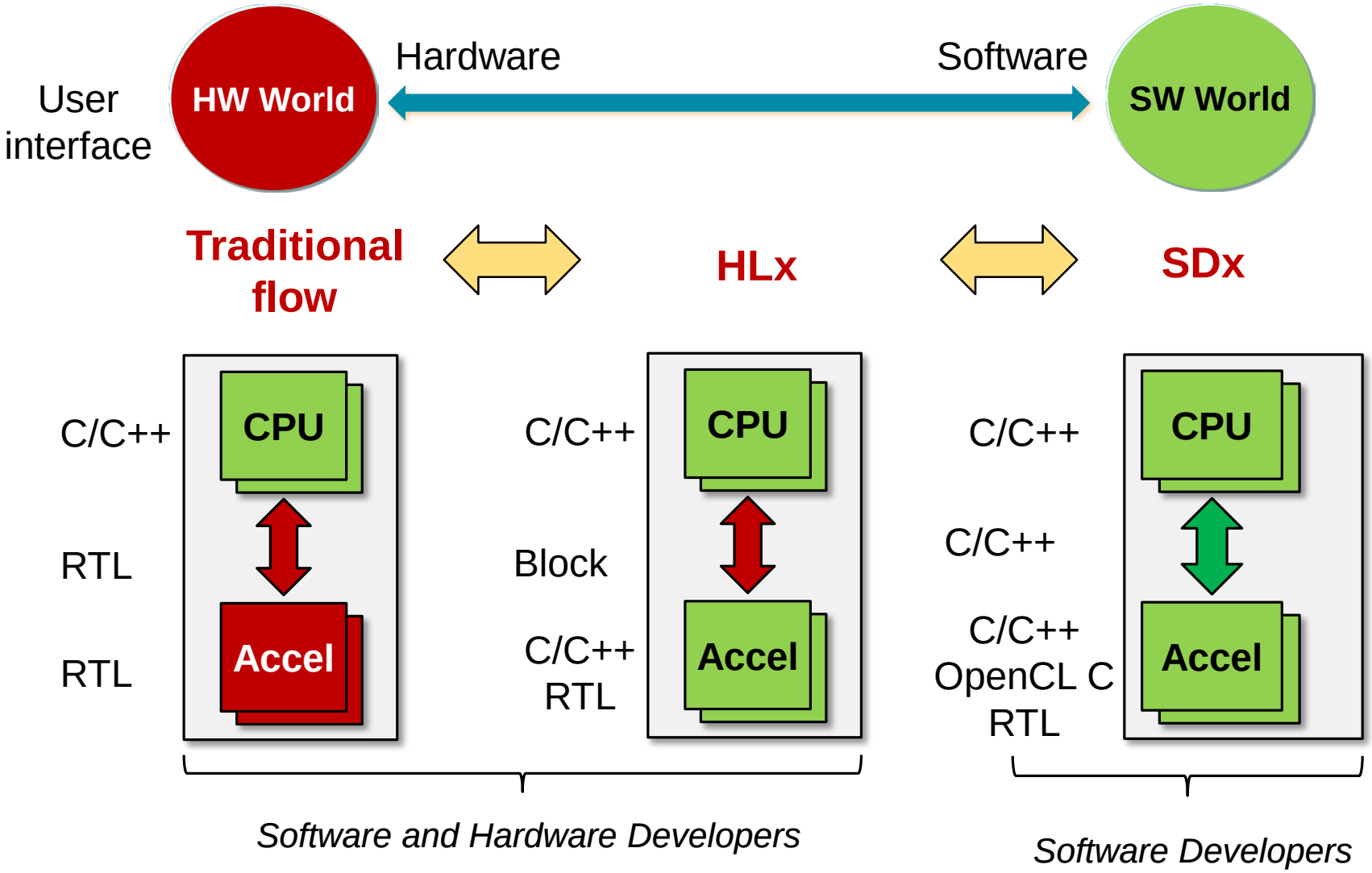
Productivity Challenges for Software

(David Thomas, Imperial College, UK)

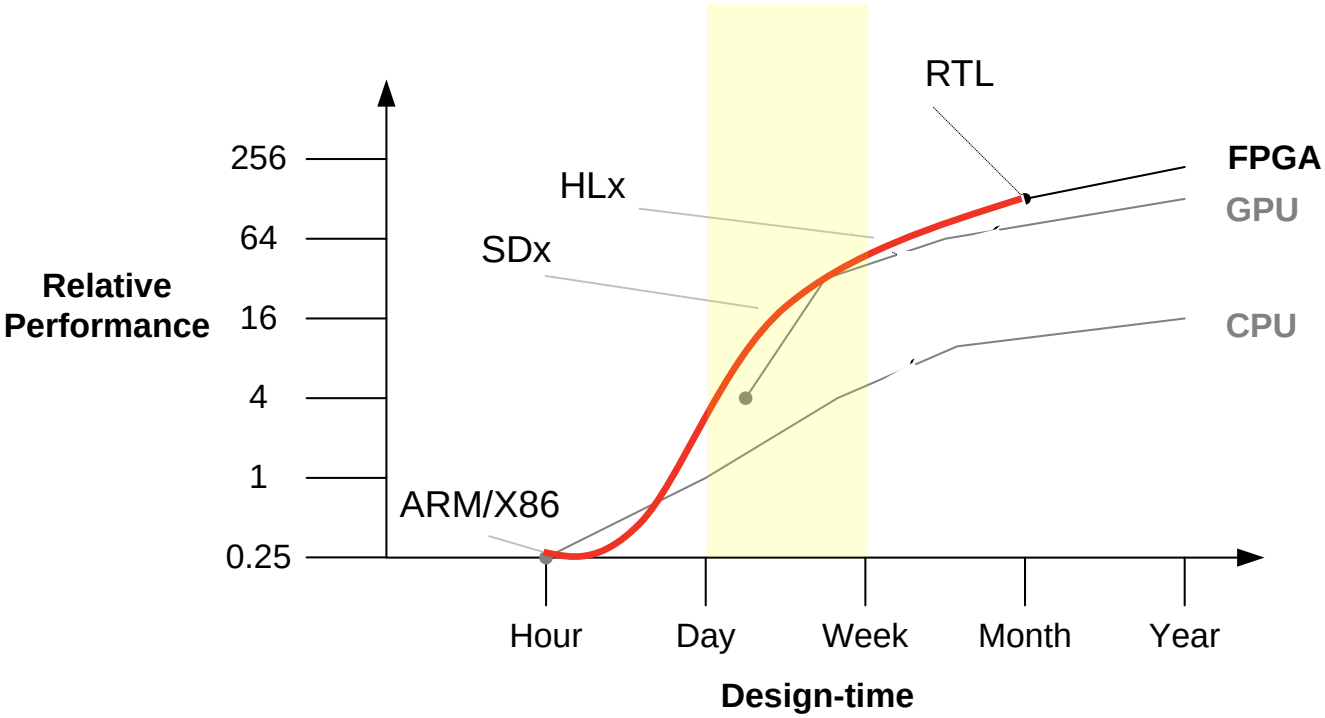


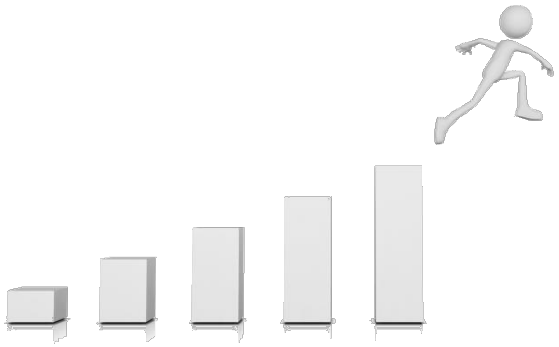
- **FPGAs provide large speed-up and power savings – *at a price!***
  - Weeks to get an initial version working
  - Multiple optimization and verification cycles to get high performance

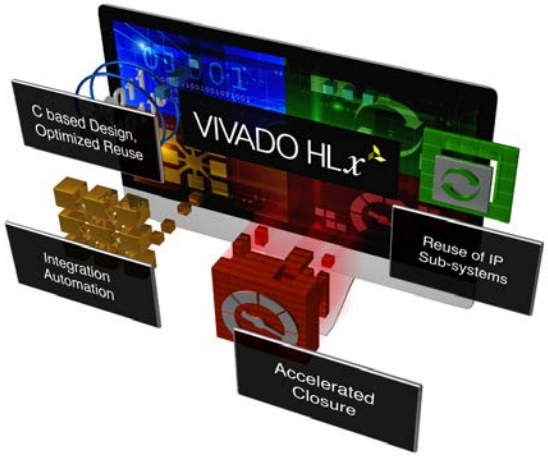
Programming Flow Evolution



Xilinx: Bridging the productivity gap



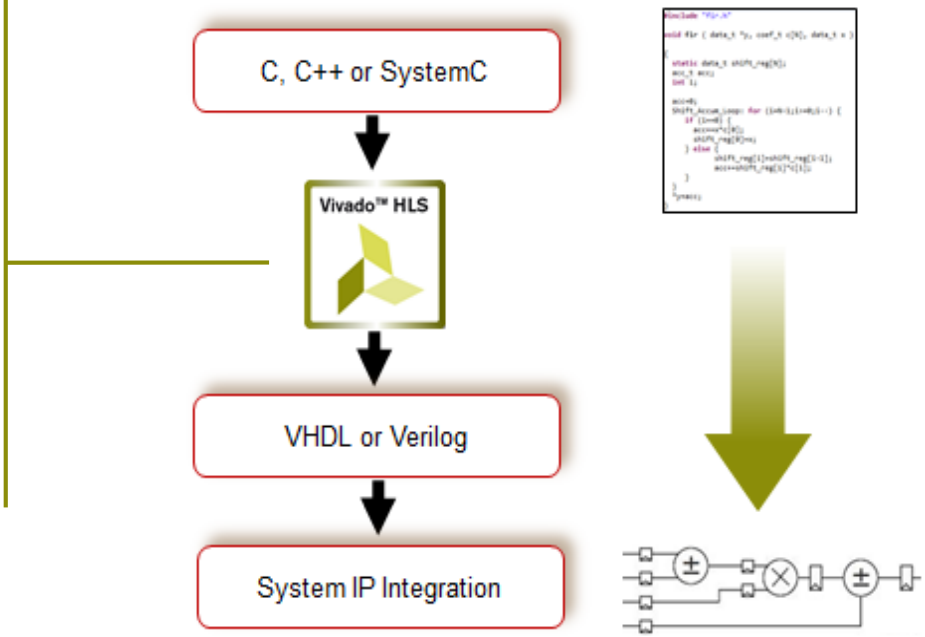




HLx: IP-Centric Design with High Level Languages

Develop New IP blocks in C/C++ Using HLS

- ***Directives / Pragmas***
- ***Constraints***
- ***Libraries***
  - *Arbitrary Precision*
  - *Video*
  - *Math*
  - *Linear algebra*
  - *IP: FFT and FIR*



- **Create IP from C/C++/System C specification**
- **Abstract algorithm verification 10,000x faster than RTL simulation**
- **Basic HW understanding needed – FPGA design experience not required**

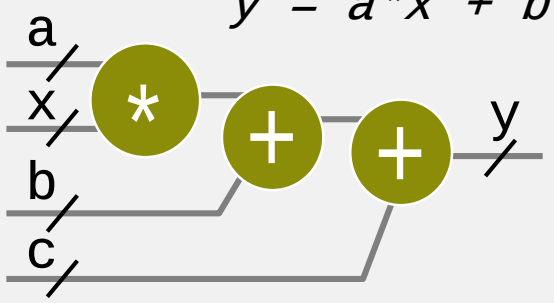
Algorithmic C to Optimized IP Generation

- **Vivado HLS adds pipeline levels to achieve high clock rates**
  - Over 300MHz can be easily achieved

Example (> 300MHz):

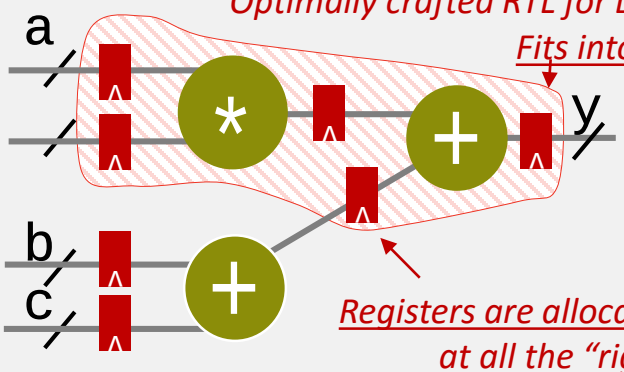
C code describes this:

```
y = a*x + b + c;
```



Vivado HLS solution:

Optimally crafted RTL for DSP blocks
Fits into a DSP48

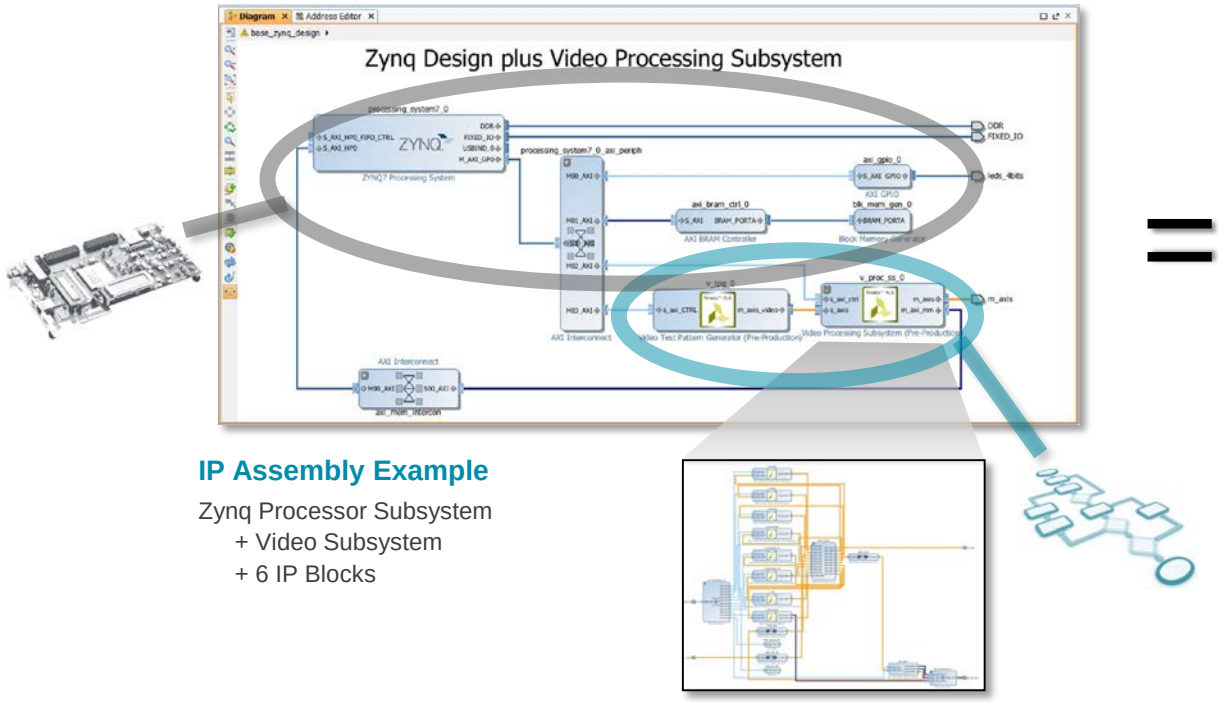


Registers are allocated by HLS at all the "right" places

- **Design Examples**
  - Chinese telecom company reaches 385MHz (wireless algorithm)
    - *"Resources utilization and performance are close to (experienced) hand-coded RTL"*
  - Application notes XAPP1236 is a 500MHz sample rate conversion filter

HLS Meets Real World Design Needs

Vivado IP Integrator for Heterogeneous System Assembly



IP Assembly Example

Zynq Processor Subsystem
+ Video Subsystem
+ 6 IP Blocks

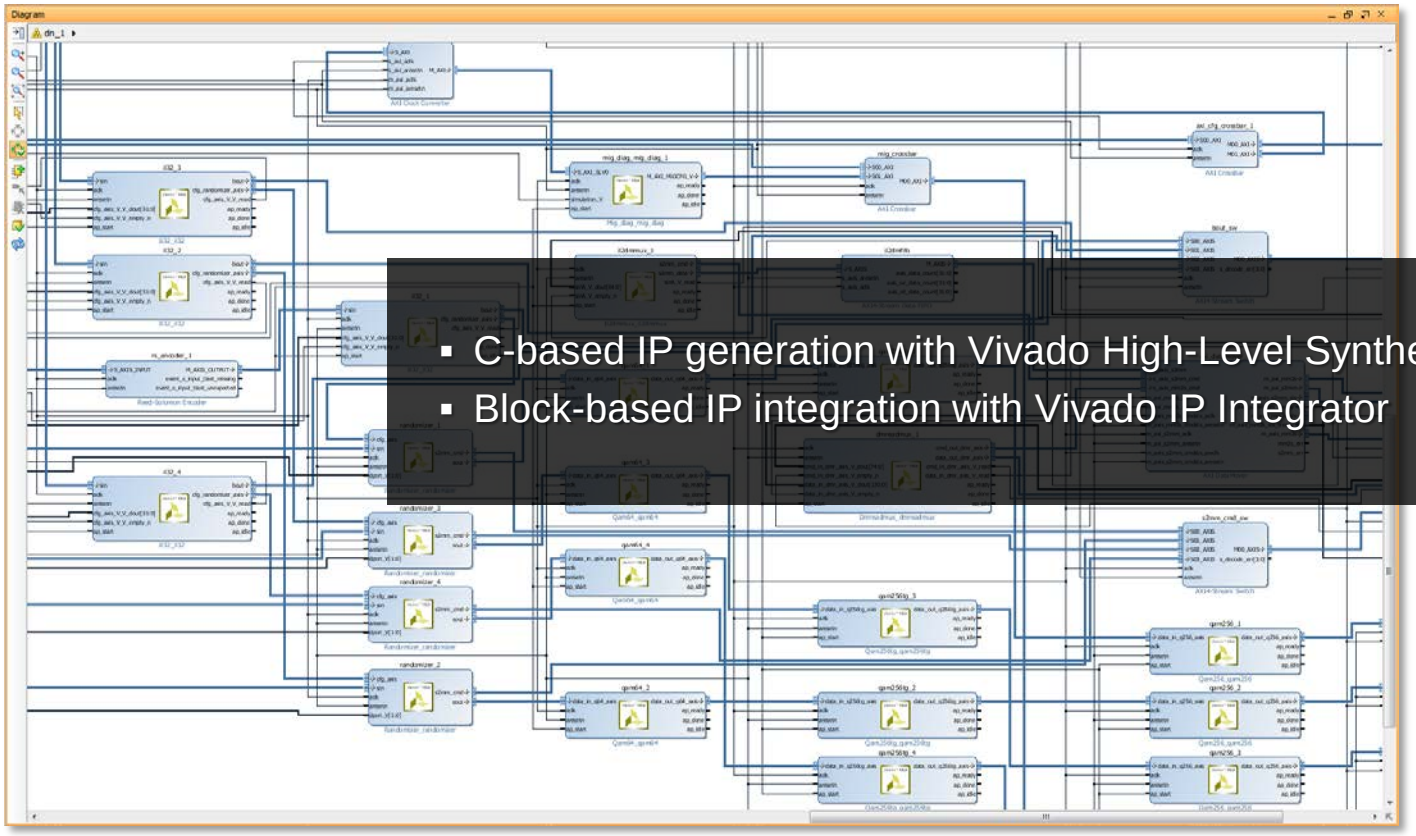
Video Processing IP Subsystem

=

4700 lines of VHDL

(top-level connectivity only)

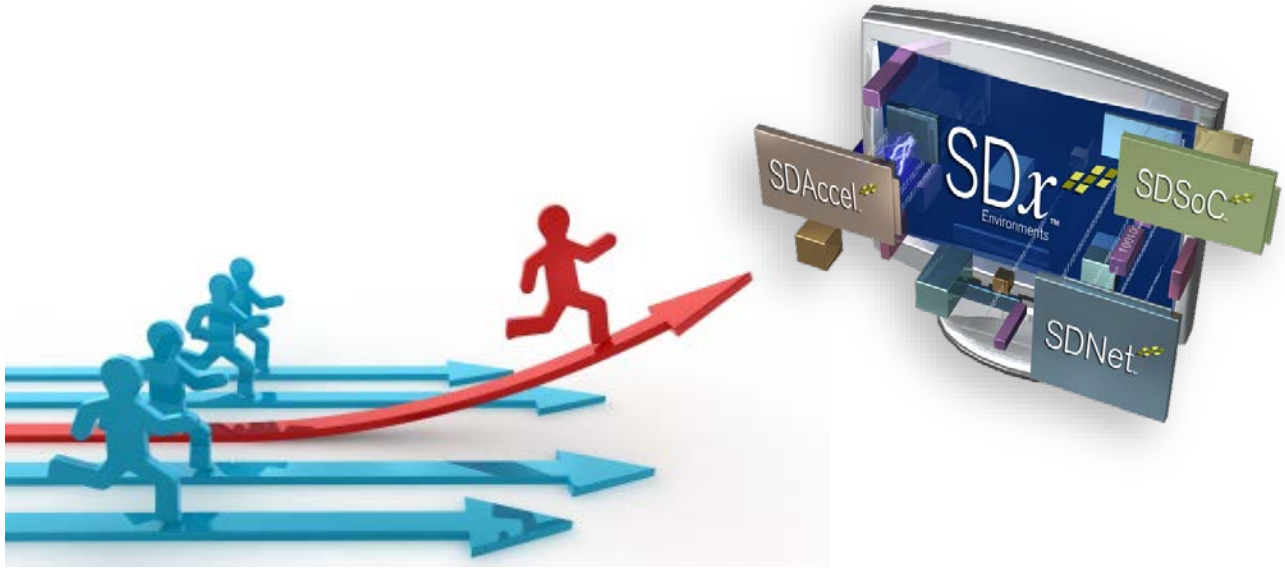
HLx Flow: Accelerated Development for SW and HW Engineers



- C-based IP generation with Vivado High-Level Synthesis
- Block-based IP integration with Vivado IP Integrator

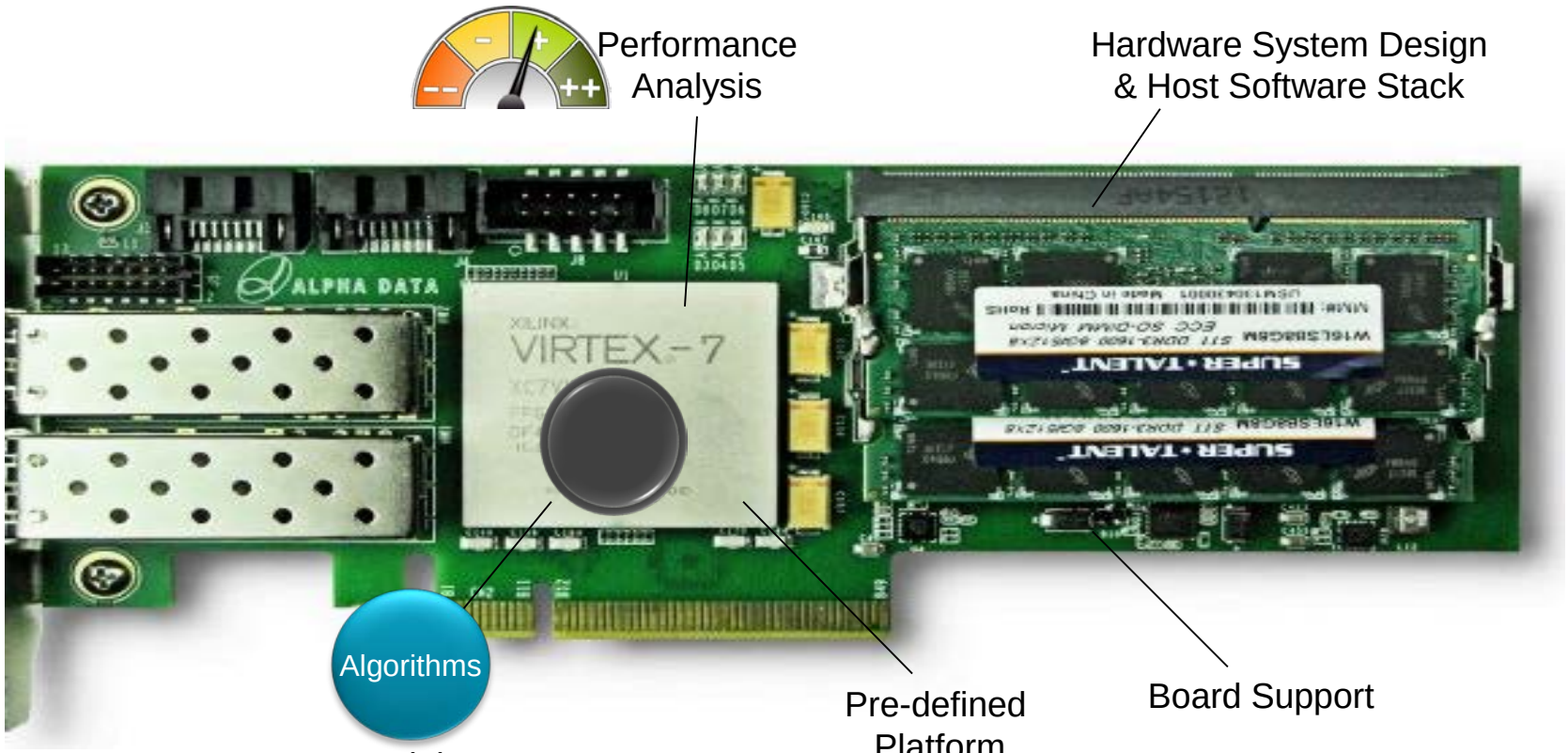
Vivado IPI and HLS: *"The combination of Vivado IPI and HLS has been invaluable to our development. The combination of these abstractions allowed us to develop our algorithms in C++ and rapidly integrate the resulting IP, saving greater than 15X in development costs versus an RTL approach."*

~Ties Bos, director of Software and FPGA at Gainspeed, Inc.

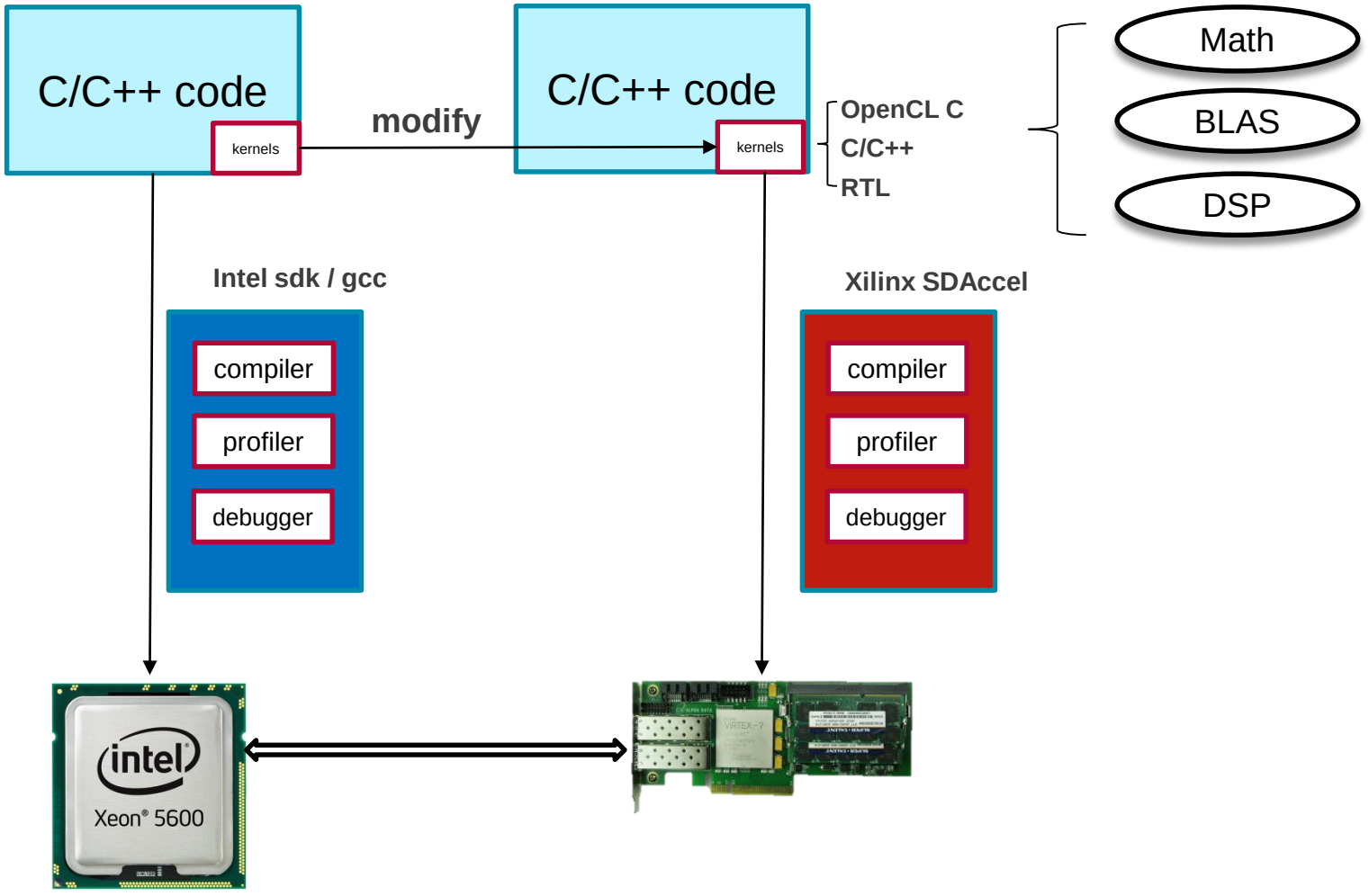


SDx: The Era of Software Defined Systems

Platforms Enable Software Defined FPGA Systems



SDAccel: CPU Programs to FPGA Acceleration

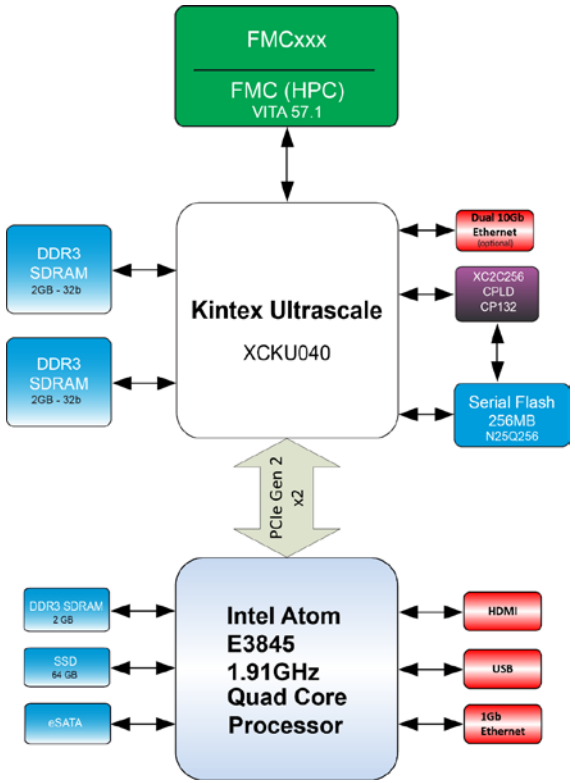


OpenCL Development Platform for SDR

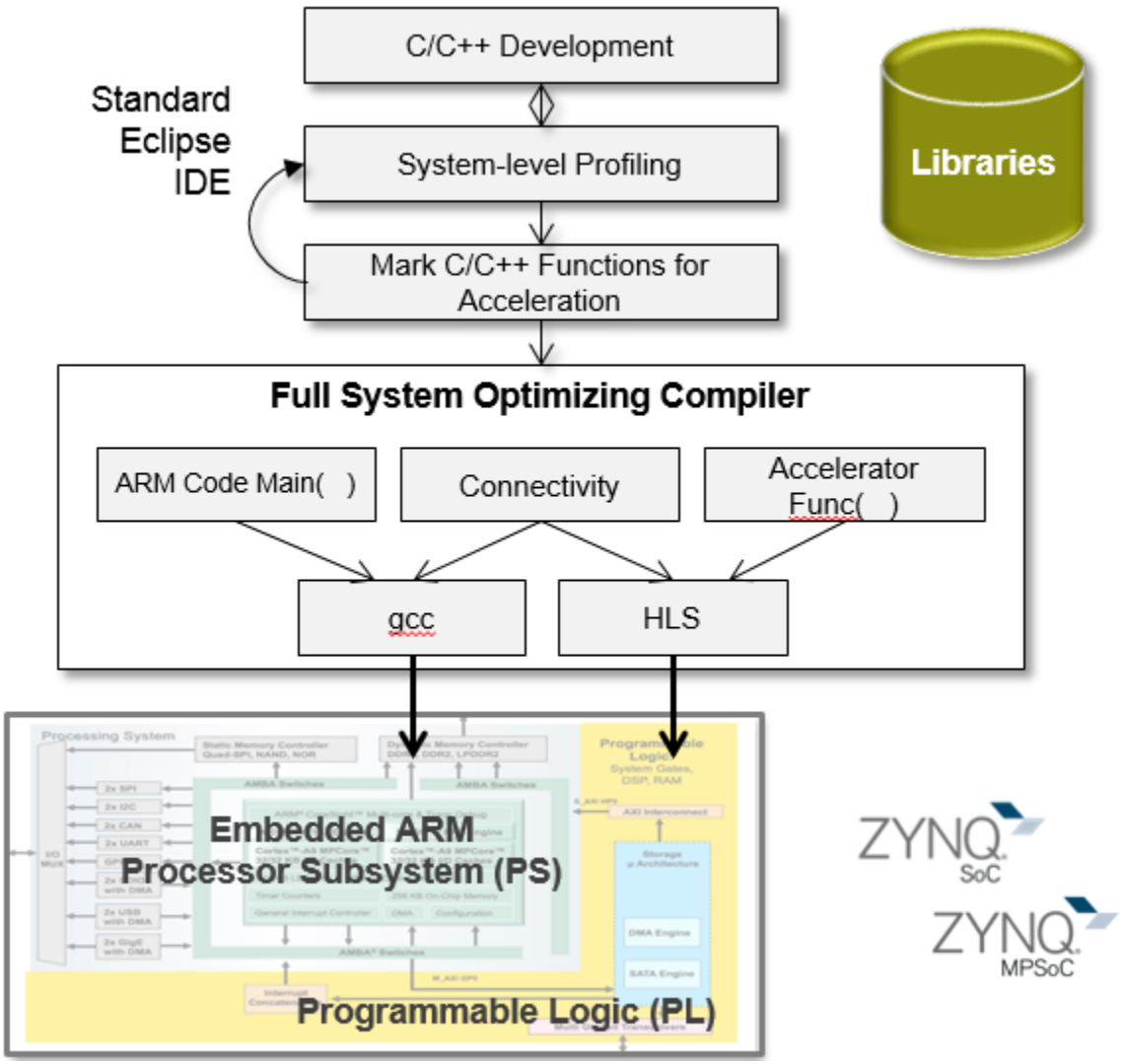
- **Development platform**
  - CPU, FPGA and Analog I/O tightly coupled
  - Self contained DAQ and processing unit
  - Lightweight, low power, portable (SWaP)

- **Programming model**
  - Develop algorithms in OpenCL C, C/C++ and RTL for FPGAs
  - Accelerate applications by integrating algorithmic kernels using OpenCL APIs

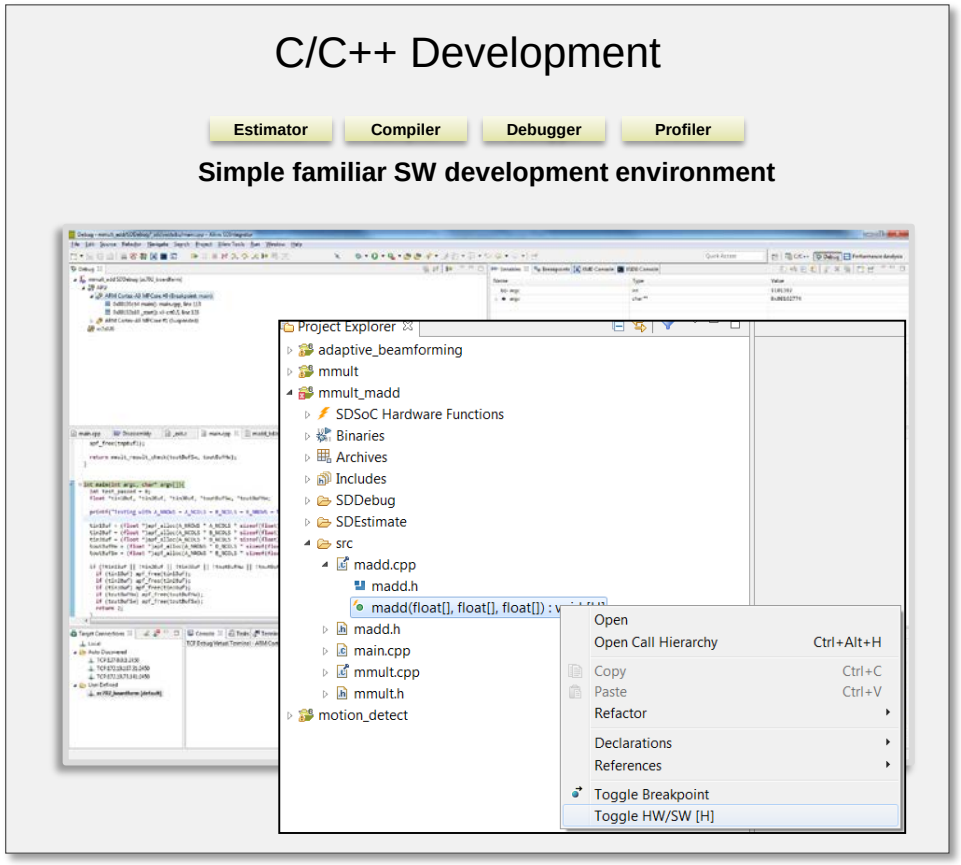
4DSP CES820



SDSoC for Zynq & MPSoC Platforms

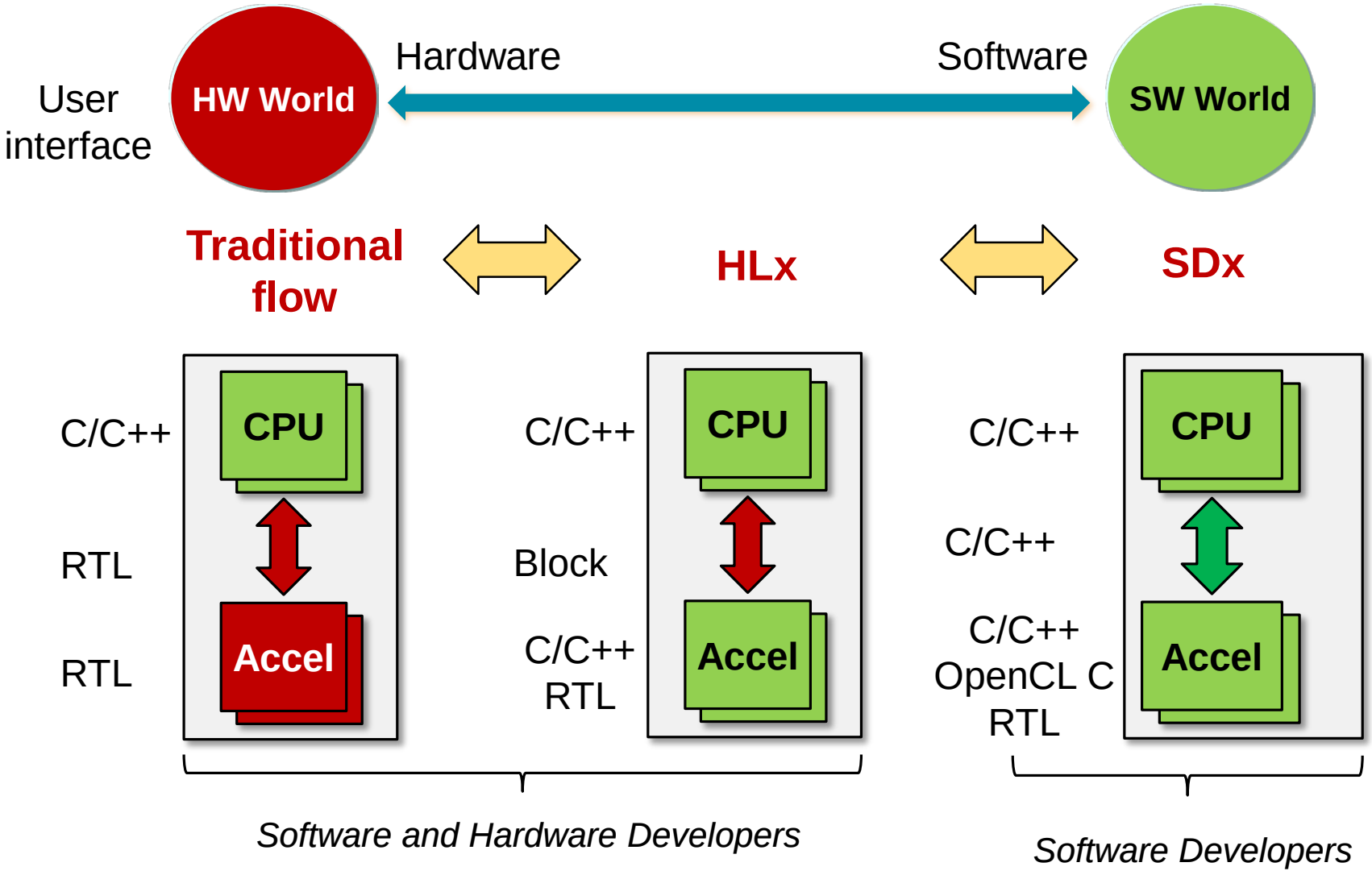


SDSoC: ASSP-like Programming Experience



- **Easy to use Eclipse IDE**
- **One click to accelerate functions in Programmable Logic (PL)**
- **Optimized libraries**
  - Xilinx, ARM and Partners
  - DSP, Video, fixed point, linear algebra, BLAS, OpenCV
- **Support for Linux, FreeRTOS, bare metal**

Programming Flow For IP-Centric and Software Defined Systems



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Thank You